**19EC2205 – DIGITAL IC APPLICATIONS**

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| **Course category:** | Program core | **Credits:** | 3 |
| **Course Type:** | Theory | **Lecture - Tutorial - Practical:** | 3 - 0– 0 |
| **Prerequisite:** | Electronic Devices, Digital System Design & Programming Skills,  | **Sessional Evaluation :****External Evaluation:****Total Marks:** | 4060100 |

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| **Course****Objectives** | Students undergoing this course are expected to understand: |
| 1. Implementing logic gates and Boolean expressions using different logic families.
2. Explain how digital circuit of large complexity can be built in a methodological way, starting from Boolean logic and applying a set of rigorous techniques.
3. Create minimal realizations of single and multiple output Boolean functions.
4. Design and analyze combinational circuits using V.H.D.L. language.
5. Design and analyze sequential circuits using V.H.D.L. language.
6. To have a profound understanding of the design of complex digital VLSI circuits and synthesis tool for hardware design.
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| **Course Outcomes** | Upon successful completion of the course, the students will be able to: |
| CO1 | Understand the process of integration and characteristics of different logic families |
| CO2 | Demonstrate knowledge of V.H.D.L. History & Language fundamentals |
| CO3 | Demonstrate knowledge of Objects inV.H.D.L |
| CO4 | Design and analyze combinational circuits for various practical problems using basic gates |
| CO5 | Design and analyze sequential circuits for various practical problems using flip flops |
| CO6 | Understand the synthesis tool for  hardware design |
| **Course****Content****Course****Content** | **UNIT – I****DIGITAL INTEGRATED CIRCUITS:** Evaluation of ICs, Advantages and classification of ICs. Digital IC characteristics, Digital IC families- DTL, HTL, ECL, MOS, CMOS, TTL-Totem-pole, Open collector and Tristate outputs and IC packaging’s.**UNIT – II****VHDL INTRODUCTION AND LANGUAGE FUNDAMENTALS:**VHDL History – **Design methodology:** - Description style, Direction of design, design flow, step in digital system design -**Hardware modeling issue:** concurrency, delays, delta time and back annotation – organization of a VHDL design file – libraries.**Language fundamentals:** Basic sequential statements – Date types – Assignment statements and operators **UNIT – III****OBJECTS IN VHDL:** Signals, Variable, constants, files-attributes of objects – VHDL package, package body and configurations – Entity declarations and statements, Logic gates using VHDL**UNIT – IV****COMBINATIONAL CIRCUIT BUILDING BLOCKS:** Multiplexers, Decoders, Encoders – Code converters and their implémentation using VHDL.**UNIT – V****SEQUENTIAL LOGIC DESIGN:** Latches and flip-flops, registers, counters (Asynchronous and synchronous) BCD, Ring and Johnson counter, FSM: Meelay and Moore-Machines and their implementation using VHDL.**UNIT – VI****VHDL SYNTHESIS:** VHDL Synthesis, Circuit Design Flow, Circuit Synthesis, Simulation, Layout, Design capture tools, Design Verification Tools. |
| **Text Books and Reference Books** | **TEXT BOOKS:**1. B.S .sonde, “Introduction to system design using ICs”, Wiley Eastern,2nd Ed, 1980
2. J Bhasker, "VHDL primer", PEARSON Education, 3rd Ed, 2015.
3. Morris Mano, "Digital Logic and Computer Design", Pearson Education, 4th Ed. 2007
4. [Pucknell Douglas A](https://www.flipkart.com/books/pucknell-douglas-a~contributor/pr?sid=bks) ," Basic VLSI Design", Prentice-Hall of India Pvt.Ltd , 3rd Ed., 2009.

**REFERENCE BOOKS:**1. Stephen Brown and zvonkovranesic, ‘Fundamentals of digital design with VHDL, TMH 3rd Ed., 2017.
2. A.P.Godse & Bakshi Digital IC Application-Technical Publications, 2014.
3. S.S. Limaye, ‘VHDL – A design oriented Approach, ‘TMH edition (2009).
 |
| **E-Resources** | 1. http://nptel.ac.in/cources
2. https:// iete-elan.ac.in
3. [https://freevideolectures.com/university/iit](https://freevideolectures.com/university/iitm)
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| Contribution of Course Outcomes towards achievement of Program Outcomes  |
|  | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
| **CO1** |  **3** | **2** | **2** | **-** | **2** | **2** | **-** | **-** | **-** | **-** | **2** | **2** | 3 | 2 |
| **CO2** | **3** | **3** | **2** | **-** | **2** | **2** | **-** | **-** | **-** | **-** | **2** | **1** | 3 | 3 |
| **CO3** | **3** | **3** | **2** |  **-** |  **1** |  **1** |  **-** |  **-** |  **-** |  **-** | **1** |  **-** |  3 |  3 |
| **CO4** | **3** | **3** | **2** | **-** | **2** | **2** | **-** | **-** |  **-** | **-** | **-** | **-** | 3 | 3 |
| **CO5** | **3** | **3** | **2** | **-** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **2** | 3 | 3 |
| **CO6** | **3** | **3** | **2** | **-** | **2** | **2** | **-** | **-** | **-** | **-** | **1** | **2** | 3 | 3 |